IN THE CLAIMS:

1. (Withdrawn) An image display device, comprising:

a pixel array portion including k (k is an integer not less than 2) signal lines, a plurality of scan lines, a plurality of pixel electrodes provided at respective regions where the respective signal lines and the respective scan lines intersect with each other, and a plurality of switching elements for driving the plurality of pixel electrodes;

a signal line driver circuit for driving the k signal lines; and

a scan line driver circuit for driving the plurality of scan lines,

wherein the signal line driver circuit includes shift registers to which m-bit (m is a natural number) digital picture signals are inputted, the number of the shift registers being a multiple of m, m x k/n (n is an integer of not less than 2) storage circuits for storing output signals of the shift registers, a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals, and k/n signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines,

wherein the plurality of D/A converter circuits are ramp type D/A converter circuits.

2. (Withdrawn) A device according to claim 1, wherein the number of the D/A converter circuits is k/n.

3. (Withdrawn) A device according to claim 1, wherein each of the plurality of ramp type D/A converter circuits comprises a bit comparison pulse width converter circuit and an analog switch.

4. (Withdrawn) A device according to claim 1, wherein the storage circuit is a latch circuit.

5. (Withdrawn) A device according to claim 4, wherein the latch circuit includes an analog switch and a holding capacitance.

6. (Withdrawn) A device according to claim 4, wherein the latch circuit includes a

clocked inverter.

7. (Withdrawn) A device according to claim 4, wherein the latch circuit includes an analog switch and a plurality of inverters.

8. (Withdrawn) A device according to claim 1, wherein a display is carried out using a liquid crystal material.

9. (Withdrawn) A device according to claim 1, wherein a display is carried out using an electroluminescence (EL) material.

10. (Withdrawn) A device according to claim 1, wherein the device is used in an electronic equipment selected from the group consisting of a portable telephone, a video camera, a personal computer, a head mount display, a television, a portable book, a CVD player, a digital camera and a projector.

11-18. (Cancelled).

19. (Currently Amended) An image display device, comprising:

a pixel array portion including a plurality of signal lines, a plurality of scan lines, a plurality of pixel electrodes provided at respective regions where the respective signal lines and the respective scan lines intersect with each other, and a plurality of switching elements for driving the plurality of pixel electrodes;

a signal line driver circuit for driving the plurality of signal lines; and

a scan line driver circuit for driving the plurality of scan lines,

wherein the signal line driver circuit includes an integral multiple of m shift registers to which m-bit (m is a natural number) digital picture signals are inputted, a plurality of storage circuits for storing output signals of the shift registers, a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals, and a plurality of signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines, and

wherein an operation in which the digital picture signals are inputted to the respective shift registers, the inputted digital picture signals are sequentially shifted in the respective shift registers in synchronization with a clock signal until they are outputted to the corresponding storage circuits, and the shifted digital picture signals are taken into the storage circuits by a latch signal while a supply of the clock signal to the respective shift registers is being stopped, is repeated n (n is an integer not less than 2) times in a time corresponding to one horizontal scan period.

20. (Previously Presented) A device according to claim 19, wherein each of the plurality of ramp type D/A converter circuits comprises a bit comparison pulse width converter circuit and an analog switch.

21. (Original) A device according to claim 19, wherein the storage circuit is a latch circuit.

22. (Original) A device according to claim 21, wherein the latch circuit includes an analog switch and a holding capacitance.

23. (Original) A device according to claim 21, wherein the latch circuit includes a clocked inverter.

24. (Original) A device according to claim 21, wherein the latch circuit includes an analog switch and a plurality of inverters.

25. (Original) A device according to claim 19, wherein a display is carried out using a liquid crystal material.

26. (Original) A device according to claim 19, wherein a display is carried out using an electroluminescence (EL) material.

27. (Previously Presented) A device according to claim 19, wherein the device is

used in an electronic equipment selected from the group consisting of a portable telephone, a video camera, a personal computer, a head mount display, a television, a portable book, a CVD player, a digital camera and a projector.

28-35. (Cancelled).

36. (Withdrawn) An image display device, comprising:

a pixel array portion including k (k is a multiple of 3) signal lines having a unit of three signal lines corresponding to R (red), G (green) and B (blue) of three primary colors of light, a plurality of scan lines, a plurality of pixel electrodes provided at respective regions where the respective signal lines and the respective scan lines intersect with each other, and a plurality of switching elements for driving the plurality of pixel electrodes;

a signal line driver circuit for driving the k signal lines; and

a scan line driver circuit for driving the plurality of scan lines,

wherein the signal line driver circuit includes shift registers to which m-bit (m is a natural number) digital picture signals are inputted respectively for the RGB, the number of the shift registers being multiple of m, m x k/n (n is a multiple of 3) storage circuits for storing output signals of the shift registers, a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals, and k/n signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines;

wherein the plurality of D/A converter circuits are ramp type D/A converter circuits.

37. (Withdrawn) A device according to claim 36, wherein the number of the D/A converter circuits is k/n.

38. (Withdrawn) A device according to claim 36, wherein each of the plurality of ramp type D/A converter circuits comprises a bit comparison pulse width converter circuit and an analog switch.

39. (Withdrawn) A device according to claim 36, wherein the storage circuit is a

latch circuit.

40. (Withdrawn) A device according to claim 39, wherein the latch circuit includes an analog switch and a holding capacitance.

41. (Withdrawn) A device according to claim 39, wherein the latch circuit includes a clocked inverter.

42. (Withdrawn) A device according to claim 39, wherein the latch circuit includes an analog switch and a plurality of inverters.

43. (Withdrawn) A device according to claim 36, wherein a display is carried out using a liquid crystal material.

44. (Withdrawn) A device according to claim 36, wherein a display is carried out using an electroluminescence (EL) material.

45. (Withdrawn) A device according to claim 36, wherein the device is used in an electronic equipment selected from the group consisting of a portable telephone, a video camera, a personal computer, a head mount display, a television, a portable book, a CVD player, a digital camera and a projector.

46-53. (Cancelled)

54. (Withdrawn) An image display device, comprising:

a pixel array portion including signal lines having a unit of three signal lines corresponding to R (red), G (green) and B (blue) of three primary colors of light, the number of the signal lines being a multiple of 3, a plurality of scan lines, a plurality of pixel electrodes provided at respective regions where the respective signal lines and the respective scan lines intersect with each other, and a plurality of switching elements for driving the plurality of pixel electrodes;

a signal line driver circuit for driving the signal lines, the number of which is the multiple of 3; and

a scan line driver circuit for driving the plurality of scan lines,

wherein the signal line driver circuit includes a multiple of m shift registers to which m-bit (m is a natural number) digital picture signals are inputted respectively for the RGB, a plurality of storage circuits for storing output signals of the shift registers, a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals, and a plurality of signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines,

one horizontal scan period includes a first, a second, and a third periods,

the digital picture signals corresponding to the R are inputted to the respective shift registers in the first period,

the digital picture signals corresponding to the G are inputted to the respective shift registers in the second period,

the digital picture signals corresponding to the B are inputted to the respective shift registers in the third period, and

in each of the three periods, an operation in which the inputted digital picture signals are sequentially shifted in the respective shift registers until they are outputted to the corresponding storage circuits, and the shifted digital picture signals are taken into the storage circuits by a latch signal, is repeated once or plural times;

wherein the plurality of D/A converter circuits are ramp type D/A converter circuits.

55. (Withdrawn) A device according to claim 54, wherein each of the plurality of ramp type D/A converter circuits comprises a bit comparison pulse width converter circuit and an analog switch.

56. (Withdrawn) A device according to claim 54, wherein the storage circuit is a latch circuit.

57. (Withdrawn) A device according to claim 56, wherein the latch circuit includes an analog switch and a holding capacitance.

58. (Withdrawn) A device according to claim 56, wherein the latch circuit includes a clocked inverter.

59. (Withdrawn) A device according to claim 56, wherein the latch circuit includes an analog switch and a plurality of inverters.

60. (Withdrawn) A device according to claim 54, wherein a display is carried out using a liquid crystal material.

61. (Withdrawn) A device according to claim 54, wherein a display is carried out using an electroluminescence (EL) material.

62. (Previously Presented) A device according to claim 54, wherein the device is used in an electronic equipment selected from the group consisting of a portable telephone, a video camera, a personal computer, a head mount display, a television, a portable book, a CVD player, a digital camera and a projector.

63-70. (Cancelled).

71. (Withdrawn) A signal line driver circuit of an image display device for driving k (k is an integer not less than 2) signal lines, the signal line driver circuit comprising:
shift registers to which m-bit (m is a natural number) digital picture signals are inputted, the number of the shift registers being a multiple of m;

m x k/n (n is an integer of not less than 2) storage circuits for storing output signals of the shift registers;

a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals; and

k/n signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines,

wherein the plurality of D/A converter circuits are ramp type D/A converter circuits.

72. (Withdrawn) A circuit according to claim 71, wherein the number of the D/A converter circuits is k/n.

73. (Withdrawn) A circuit according to claim 71, wherein each of the plurality of ramp type D/A converter circuits comprises a bit comparison pulse width converter circuit and an analog switch.

74. (Withdrawn) A circuit according to claim 71, wherein the storage circuit is a latch circuit.

75. (Withdrawn) A circuit according to claim 74, wherein the latch circuit includes an analog switch and a holding capacitance.

76. (Withdrawn) A circuit according to claim 74, wherein the latch circuit includes a clocked inverter.

77. (Withdrawn) A circuit according to claim 74, wherein the latch circuit includes an analog switch and a plurality of inverters.

78. (Withdrawn) A circuit according to claim 71, wherein the driver circuit of the image display device is formed of a polysilicon thin film transistor.

79. (Withdrawn) A circuit according to claim 71, wherein the driver circuit of the image display device is formed of a single crystal transistor.

80. (Currently Amended) A signal line driver circuit of an image display device for driving a plurality of signal lines, the signal line driver circuit comprising:

an integral multiple of m shift registers to which m-bit (m is a natural number) digital picture signals are inputted;

a plurality of storage circuits for storing output signals of the shift registers;

a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals; and

a plurality of signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines,

wherein an operation in which the digital picture signals are inputted to the respective shift registers, the inputted digital picture signals are sequentially shifted in the respective shift registers in synchronization with a clock signal until they are outputted to the corresponding storage circuits, and the shifted digital picture signals are taken into the storage circuits by a latch signal while a supply of the clock signal to the respective shift registers is being stopped, is repeated n (n is an integer not less than 2) times in a time corresponding to one horizontal scan period.

81. (Previously Presented) A circuit according to claim 80, wherein each of the plurality of ramp type D/A converter circuits comprises a bit comparison pulse width converter circuit and an analog switch.

82. (Original) A circuit according to claim 80, wherein the storage circuit is a latch circuit.

83. (Original) A circuit according to claim 82, wherein the latch circuit includes an analog switch and a holding capacitance.

84. (Original) A circuit according to claim 82, wherein the latch circuit includes a clocked inverter.

85. (Original) A circuit according to claim 82, wherein the latch circuit includes an analog switch and a plurality of inverters.

86. (Original) A circuit according to claim 80, wherein the driver circuit of the image display device is formed of a polysilicon thin film transistor.

87. (Original) A circuit according to claim 80, wherein the driver circuit of the image display device is formed of a single crystal transistor

88. (Withdrawn) A signal line driver circuit of an image display device for driving signal lines having a unit of three signal lines corresponding to R (red), G (green) and B (blue) of three primary colors of light, the number of the signal lines being a multiple of 3, the signal line driver circuit comprising:

shift registers to which m-bit (m is a natural number) digital picture signals are inputted respectively for the RGB, the number of the shift registers being a multiple of m;

m x k/n (n is a multiple of 3) storage circuits for storing output signals of the shift registers;

a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals; and

k/n signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines;

wherein the plurality of D/A converter circuits are ramp type D/A converter circuits.

89. (Withdrawn) A circuit according to claim 88, wherein the number of the D/A converter circuits is k/n.

90. (Withdrawn) A circuit according to claim 88, wherein each of the plurality of ramp type D/A converter circuits comprises a bit comparison pulse width converter circuit and an analog switch.

91. (Withdrawn) A circuit according to claim 88, wherein the storage circuit is a latch circuit.

92. (Withdrawn) A circuit according to claim 91, wherein the latch circuit includes an analog switch and a holding capacitance.

93. (Withdrawn) A circuit according to claim 91, wherein the latch circuit includes a

clocked inverter.

94. (Withdrawn) A circuit according to claim 91, wherein the latch circuit includes an analog switch and a plurality of inverters.

95. (Withdrawn) A circuit according to claim 88, wherein the driver circuit of the image display device is formed of a polysilicon thin film transistor.

96. (Withdrawn) A circuit according to claim 88, wherein the driver circuit of the image display device is formed of a single crystal transistor.

97. (Withdrawn) A signal line driver circuit of an image display device for driving signal lines having a unit of three signal lines corresponding to R (red), G (green) and B (blue) of three primary colors of light, the number of the signal lines being a multiple of 3, the signal line driver circuit comprising:

a multiple of m shift registers to which m-bit (m is a natural number) digital picture signals are inputted respectively for the RGB;

a plurality of storage circuits for storing output signals of the shift registers;

a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals; and

a plurality of signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines, wherein

one horizontal scan period includes a first, a second, and a third periods,

the digital picture signals corresponding to the R are inputted to the respective shift registers in the first period,

the digital picture signals corresponding to the G are inputted to the respective shift registers in the second period,

the digital picture signals corresponding to the B are inputted to the respective shift registers in the third period, and

in each of the three periods, an operation in which the inputted digital picture signals are sequentially shifted in the respective shift registers until they are outputted to the

corresponding storage circuits, and the shifted digital picture signals are taken into the storage circuits by a latch signal, is repeated once or plural times;

wherein the plurality of D/A converter circuits are ramp type D/A converter circuits.

98. (Withdrawn) A circuit according to claim 97, wherein each of the plurality of ramp type D/A converter circuits comprises a bit comparison pulse width converter circuit and an analog switch.

99. (Withdrawn) A circuit according to claim 97, wherein the storage circuit is a latch circuit.

100. (Withdrawn) A circuit according to claim 99, wherein the latch circuit includes an analog switch and a holding capacitance.

101. (Withdrawn) A circuit according to claim 99, wherein the latch circuit includes a clocked inverter.

102. (Withdrawn) A circuit according to claim 99, wherein the latch circuit includes an analog switch and a plurality of inverters.

103. (Withdrawn) A circuit according to claim 97, wherein the driver circuit of the image display device is formed of a polysilicon thin film transistor.

104. (Withdrawn) A circuit according to claim 97, wherein the driver circuit of the image display device is formed of a single crystal transistor.

105. (Currently Amended) An image display device, comprising:

a pixel array portion including k (k is an integer not less than 2) signal lines, a plurality of scan lines, a plurality of pixel electrodes provided at respective regions where the respective signal lines and the respective scan lines intersect with each other, and a plurality of switching elements for driving the plurality of pixel electrodes;

a signal line driver circuit for driving the k signal lines; and

a scan line driver circuit for driving the plurality of scan lines,

wherein the signal line driver circuit includes shift registers to which m-bit (m is a natural number) digital picture signals are inputted, the number of the shift registers being an integral multiple of m, m x k/n (n is an integer of not less than 2) storage circuits for storing output signals of the shift registers, a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals, and k/n signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines[[.]], and

wherein an operation in which the digital picture signals are inputted to the respective shift registers, the inputted digital picture signals are sequentially shifted in the respective shift registers in synchronization with a clock signal until they are outputted to the corresponding storage circuits, and the shifted digital picture signals are taken into the storage circuits by a latch signal while a supply of the clock signal to the respective shift registers is being stopped, is repeated j (j is an integer not less than 2) times in a time corresponding to one horizontal scan period.

106. (Previously presented) A device according to claim 105, wherein the number of the D/A converter circuits is k/n.

107. (Previously presented) A device according to claim 105, wherein each of the plurality of ramp type D/A converter circuits comprises a bit comparison pulse width converter circuit and an analog switch.

108. (Previously presented) A device according to claim 105, wherein the storage circuit is a latch circuit.

109. (Previously presented) A device according to claim 108, wherein the latch circuit includes an analog switch and a holding capacitance.

110. (Previously presented) A device according to claim 108, wherein the latch

circuit includes a clocked inverter.

111. (Previously presented) A device according to claim 108, wherein the latch circuit includes an analog switch and a plurality of inverters.

112. (Previously presented) A device according to claim 105, wherein a display is carried out using a liquid crystal material.

113. (Previously presented) A device according to claim 105, wherein a display is carried out using an electroluminescence (EL) material.

114. (Previously presented) A device according to claim 105, wherein the device is used in an electronic equipment selected from the group consisting of a portable telephone, a video camera, a personal computer, a head mount display, a television, a portable book, a CVD player, a digital camera and a projector.

115. (Currently Amended) A signal line driver circuit of an image display device for driving k (k is an integer not less than 2) signal lines, the signal line driver circuit comprising:

shift registers to which m-bit (m is a natural number) digital picture signals are inputted, the number of the shift registers being an integral multiple of m;

m x k/n (n is an integer of not less than 2) storage circuits for storing output signals of the shift registers;

a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals; and

k/n signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines[[.]],

wherein an operation in which the digital picture signals are inputted to the respective shift registers, the inputted digital picture signals are sequentially shifted in the respective shift registers in synchronization with a clock signal until they are outputted to the corresponding storage circuits, and the shifted digital picture signals are taken into the storage circuits by a latch signal while a supply of the clock signal to the respective shift registers is

being stopped, is repeated j (j is an integer not less than 2) times in a time corresponding to one horizontal scan period.

116. (Previously presented) A circuit according to claim 115, wherein the number of the D/A converter circuits is k/n.

117. (Previously presented) A circuit according to claim 115, wherein each of the plurality of ramp type D/A converter circuits comprises a bit comparison pulse width converter circuit and an analog switch.

118. (Previously presented) A circuit according to claim 115, wherein the storage circuit is a latch circuit.

119. (Previously presented) A circuit according to claim 118, wherein the latch circuit includes an analog switch and a holding capacitance.

120. (Previously presented) A circuit according to claim 118, wherein the latch circuit includes a clocked inverter.

121. (Previously presented) A circuit according to claim 118, wherein the latch circuit includes an analog switch and a plurality of inverters.

122. (Previously presented) A circuit according to claim 115, wherein the driver circuit of the image display device is formed of a polysilicon thin film transistor.

123. (Previously presented) A circuit according to claim 115, wherein the driver circuit of the image display device is formed of a single crystal transistor.